IN THE CLAIMS:

1. A method of fabricating an integrated circuit, comprising the steps of:

providing a semiconductor body having a top metal interconnect level formed thereon, said top metal interconnect level having a first and a second metal interconnect line;

depositing a material over said top metal interconnect level;

patterning and etching said material to expose a portion of said top metal interconnect level; and

forming a capacitor on said exposed portion of said top metal interconnect level, wherein said first metal interconnect line is protected by said material during said step of forming said capacitor.

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2. The method of claim 1, wherein the step of forming said capacitor comprises the steps of:

depositing a bottom electrode material on said exposed portion of said top metal interconnect level;

forming a capacitor dielectric over said bottom electrode material;

depositing a top electrode material over said capacitor dielectric; and

patterning and etching said top electrode material, said capacitor dielectric, and said bottom electrode material to form said capacitor.

3. The method of claim 2, further comprising the steps of:

forming a protective overcoat over said top electrode and said top metal interconnect level;

forming a cap partially over said protective overcoat, said cap electrically connecting said top electrode material and said second metal interconnect line.

4. The method of claim 1, wherein said bottom electrode material and said top electrode material each comprise TaN.

5. The method of claim 1, wherein said bottom electrode material and said top electrode material each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ir, Ru, and Ta.

6. The method of claim 1, wherein said capacitor dielectric layer comprises tantalum-oxide.

7. The method of claim 1, wherein said capacitor dielectric layer comprises hafnium-oxide or silicon nitride.

8. The method of claim 1, wherein said first and second metal interconnect lines comprise copper.

9. An integrated circuit comprising:

a topmost metal interconnect level located over a semiconductor body, said topmost metal interconnect level comprising a first and a second metal interconnect line;

a decoupling capacitor located over said topmost metal interconnect level, wherein a bottom electrode of said decoupling capacitor is electrically connected to said first metal interconnect line;

a protect layer on said second metal interconnect line;

an etchstop layer over said protect layer;

a protective overcoat over said etchstop layer; and

an aluminum cap layer located partially over said protective overcoat and electrically connecting a top electrode of said decoupling capacitor to said second copper interconnect line.

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~~11~~. The integrated circuit of claim 9, wherein said top electrode and said bottom electrode comprise TaN.

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~~12~~. The integrated circuit of claim 9, wherein said top electrode and said bottom electrode each comprise one or more layers of material selected from the group consisting of TaN, TiN, Ir, Ru, and Ta.

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~~13~~. The integrated circuit of claim 9, wherein said capacitor dielectric comprises tantalum-oxide.

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~~14~~. The method of claim ~~13~~, wherein said step of forming a capacitor dielectric comprises the steps of:

depositing a layer of tantalum-oxide over said bottom electrode; and

annealing said layer of tantalum-oxide in oxygen to reduce impurities and increase the oxygen content.

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~~15~~. The integrated circuit of claim 9, wherein said capacitor dielectric comprises hafnium-oxide or silicon nitride.

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~~16~~. The integrated circuit of claim 9, wherein said first and second metal interconnect lines comprise copper.